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(71) Applicant: **MOTOROLA, INC.**
Schaumburg, IL 60196 (US)

(72) Inventor: **Naji, Peter K.**
Phoenix, Arizona 85048 (US)

(74) Representative:
Gibson, Sarah Jane et al
Motorola
European Intellectual Property Operations
Midpoint
Alencon Link
Basingstoke, Hampshire RG21 7PL (GB)

(54) Processing equipment with embedded MRAMS including dual read ports

(57) Processing equipment with embedded MRAMs, and a method of fabricating, including a data processing device (10) fabricated on a semiconductor chip with MRAM cells fabricated on the chip to form one to all of the memories on the chip. Also included is a dual bank memory (31,32) in communication with the data processing (10) device and circuitry coupled to the data processing device and the dual bank memory for providing simultaneous read access to the dual bank memory.

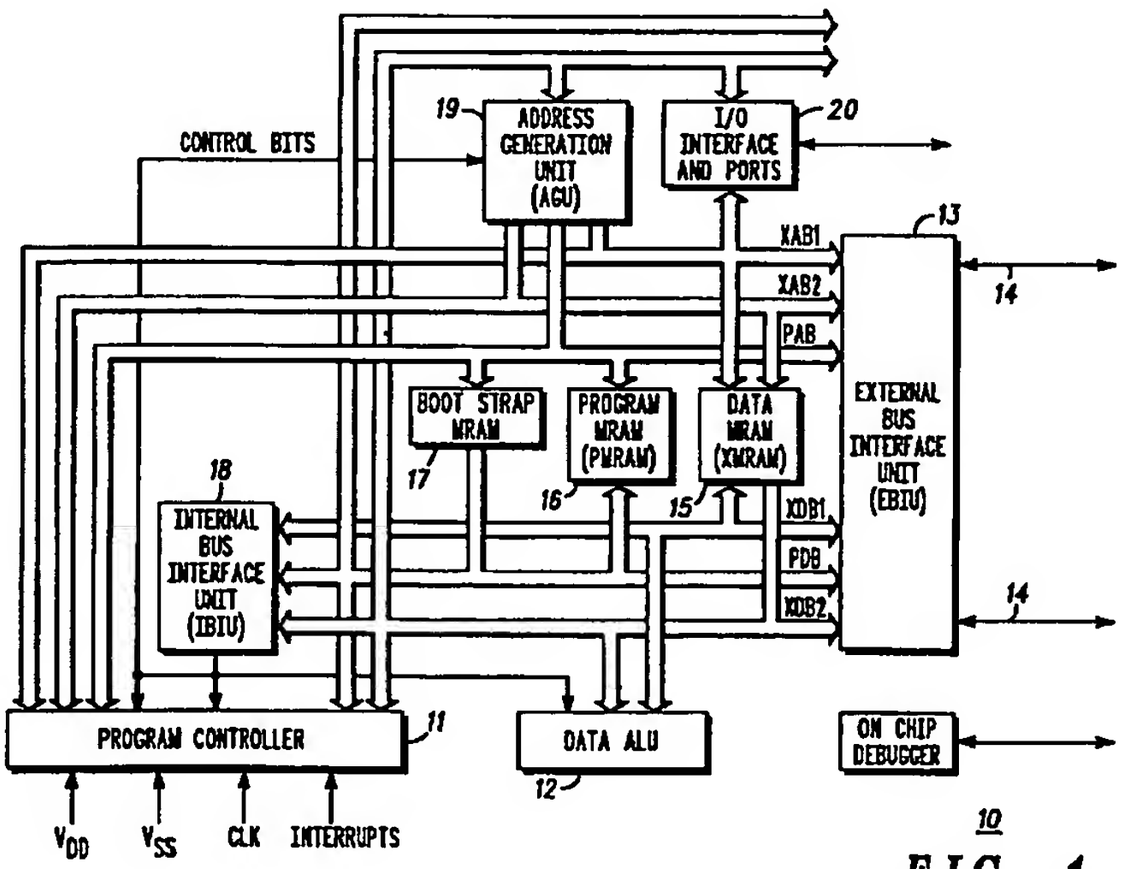

FIG. 1

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Description

Field of the Invention

[0001] The present invention pertains to memories in data processing equipment.

Background of the Invention

[0002] Many different types of data processing equipment are manufactured and used in the present day market, such as microprocessors, micro controllers, digital signal processors (DSP), or the like. All of these types of data processing equipment use a variety of memories, such as a data memory, a program or instruction memory, a boot memory, a cash memory, controlling shift registers, etc. At the present time, all of these various memories use memory devices such as DRAMs, SRAMs, flash memories, ROMs, PROMs, etc. For example, data and program memories typically use SRAMs, ROMs, or flash memories for the storage of data and operating programs. While SRAMs are very high speed, they are volatile, which means that they loose the data when power is removed and, therefore, their use is very limited. Other types of memories are generally slower and many of them require much additional circuitry, which renders them costly and relatively large.

[0003] It would be desirable, therefore, to provide data processing equipment which overcomes these drawbacks.

[0004] It is an object of the present invention to provide new and improved memories in data processing equipment.

[0005] It is another object of the present invention to provide new and improved memories in data processing equipment which is as fast as SRAMs but non-volatile.

[0006] It is still another object of the present invention to provide new and improved memories in data processing equipment with dual read ports to further enhance the speed of the equipment.

Summary of the Invention

[0007] The above problems and others are at least partially solved and the above objects and others are realized in processing equipment with embedded MRAMs and a method of fabricating the equipment. The data processing equipment includes a data processing device fabricated on a semiconductor chip with MRAM cells fabricated on the chip to form one to all of the memories on the chip, including a data memory, a program or instruction memory, a boot memory, a cash memory, and controlling shift registers in communication with the data processing device.

[0008] Also, in a specific embodiment, the data processing equipment includes a dual bank memory in communication with the data processing device and circuitry coupled to the data processing device and the dual bank memory for providing simultaneous read access to the dual bank memory.

Brief Description of the Drawings

[0009] Referring to the drawings:

FIG. 1 is a block diagram of data processing equipment including embedded MRAMs in accordance with the present invention;
FIG. 2 is a block diagram of a dual port MRAM memory in conjunction with the present invention; and
FIGS. 3, 4, and 5 are schematic diagrams of portions of a block in the diagram of FIG. 2.

Description of the Preferred Embodiments

[0010] Turning now to FIG. 1, a simplified block diagram of a data processor 10 including embedded MRAM memories in accordance with the present invention. For purposes of this disclosure the term "MRAM", stands for Magnetic Random Access Memory and is defined herein as including any of the relatively recently developed thin film magnetic memory cells including magnetic tunneling junctions (MTJ), giant magnetic resonance cells (GMR), and thin magnetic film junctions separated by an electrical conductor or an electrical insulator, etc. Examples of MRAMs of each of these types are described in the patent applications set forth below, all of which are incorporated herein by reference. U.S. Patent No. 5,702,831, entitled "Ferromagnetic GMR Material", issued 30 December 1997; U.S. Patent No. 5,732,016, entitled "Memory Cell Structure in a Magnetic Random Access Memory and a Method for Fabricating Thereof", issued 24 March 1998; and U.S. Patent No. 5,702,831, entitled "Multi-Layer Magnetic Tunneling Junction Memory Cells", issued 31 March 1998.

[0011] Data processor 10 can be, for example, any of the various processing devices fabricated on a semiconductor chip, such as a microprocessor, a micro controller, a digital signal processor (DSP), or the like. Data processor 10 includes (among other things) a program controller 11, which receives various inputs, including power sources Vdd and Vss, a clock input (clk) and various "interrupts" of a working program. Data processor 10 also includes a data logic unit (ALU) 12 which utilizes the data to perform various operations, as is known in the art.

[0012] An external bus interface unit (EBIU) 13 receives data and other instructions (e.g. 'read' or 'write' instructions) from an external source by way of a bus 14 that is connected to external equipment (not shown). Interface unit 13 is connected by way of various internal buses to a data MRAM 15, a program MRAM 16 and a boostrap MRAM 17. Each of these units performs tasks

well known in the art as, for example, data MRAM 15 stores data introduced by way of interface bus 13, program MRAM 16 contains programs which dictate or control the operation of data processor 10, and bootstrap MRAM 17 controls the start-up of data processor 10. Interface bus 13 is also connected to program controller 11 and an internal bus interface unit (IBIU) 18. Various other units are coupled into the buses and network to perform various tasks, such as an address generating unit (AGU) 19 and I/O (input/output) interface and ports 20.

[0013] All of the described units and interfaces are generally fabricated on a single semiconductor chip (although some minor components may be connected off chip), including the various memories described, along with additional memories in some other specific data processors. In data processor 10, all of the various memories are some type of MRAM, fabricated as described in any of the above referenced patent applications. Since all of the embedded memories (e.g. data MRAM 15, program MRAM 16, and bootstrap MRAM 17) are of the same type, the fabrication or manufacturing process is greatly simplified. Further, the speed of data processor 10 can be substantially enhanced because the speed of the MRAMs is as fast as SRAMs but non-volatile. Because SRAMs are volatile, they can not be used where permanent or semipermanent storage is required (e.g. program memories) and, thus, slower memories must be used in many of the various positions, which substantially slows the operation. Also, MRAMs make it possible such that the same processor can be used for development and for production. Otherwise, a flash based or ROM based processor is used for development and later the flash/ROM is converted to SRAM for production.

[0014] Turning now to FIG. 2, a dual port MRAM 30 is illustrated in simplified block form. MRAM 30 includes a left bank 31 (also referred to as a low address space) and a right bank 32 (also referred to as a high address space) of MRAM cells. Each of banks 31 and 32 include an array of MRAM cells with each MRAM cell being individually addressable by row and column. A row source 35 is coupled through a row multiplexer 36 to one end of the rows of MRAM cells in left bank 31 and through a row multiplexer 37 to one end of the rows of MRAM cells in right bank 32. Left bank 31 has a row sink 40 connected to the other end of the rows of MRAM cells and right bank 32 has a row sink 41 connected to the other end of the rows of MRAM cells. Row multiplexer 36 receives address inputs by way of a row decoder 44 which receives an address on parallel lines, designated a_1j, from an address space selector 45. Similarly, row multiplexer 37 receives address inputs by way of a row decoder 46 which receives an address on parallel lines, designated a_2j, from address space selector 45.

[0015] A column or bitline source/sink 51 is coupled through a column multiplexer 52 to one end (the lower end in FIG. 2) of the columns of MRAM cells in left bank 31 and the other end of the columns of cells in left bank 31 is connected to a second column or bitline source/sink 53. Similarly, a column or bitline source/sink 54 is coupled through a column multiplexer 55 to one end (the lower end in FIG. 2) of the columns of MRAM cells in right bank 32 and the other end of the columns of cells in right bank 32 is connected to a second column or bitline source/sink 56. Column multiplexer 52 receives address inputs by way of a column decoder 57 which receives an address on parallel lines, designated $a_1(i-j)$, from address space selector 45. Similarly, column multiplexer 55 receives address inputs by way of a column decoder 58 which receives an address on parallel lines, designated $a_2(i-j)$, from address space selector 45.

[0016] The data output from MRAM 30 is available at dual ports or lines, designated XDB_1 and XDB_2. Data from left bank 31 is supplied in parallel by way of column multiplexer 52 through a plurality of amplifiers 60 and to first and/or second controlled output buffers 61 and 62. Controlled output buffer 61 supplies output data to output line XDB_1 and controlled output buffer 62 supplies output data to output line XDB_2. In a similar fashion, data from right bank 32 is supplied in parallel by way of column multiplexer 55 through a plurality of amplifiers 63 and to first and/or second controlled output buffers 64 and 65. Controlled output buffer 64 supplies output data to output line XDB_1 and controlled output buffer 65 supplies output data to output line XDB_2. Controlled output buffers 61 and 64 are turned ON or activated by means of an enable signal supplied by a unit, designated 70, on a lead designated 71. Controlled output buffers 62 and 65 are turned ON or activated by means of an enable signal supplied by unit 70 on a lead designated 72.

[0017] Unit 70 is illustrated as a separate block in FIG. 2 but it can be considered for all practical purposes a portion of address space selector 45. Assuming, for sake of explanation, that MRAM 30 is incorporated in a digital signal processor (DSP), unit 70 receives two processing signals, designated XR_1P and XR_2P, and a read/write signal from the DSP core.(not shown). Also, address space selector 45 receives two input signals, designated XAb_1 and XAb_2, and supplies signals a_1i and a_2i to row decoders 44 and 46 and to column decoders 57 and 58. Further, unit 70 generates six signals, designated XR_1, XR_2, XR_3a, XR_3b, XR_4a, and XR_4b, from processing signals XR_1P and XR_2P and a "read" signal which it supplies internally to address space selector 45. Address space selector 45 then uses the six signals from unit 70 to generate address signals a_1i and a_2i from input signals XAb_1 and XAb_2.

[0018] Turning now to FIG. 3, a schematic diagram of a logic circuit 75 of unit 70 is illustrated. Logic circuit 75 generates four different timing signals A, B, C, and D from input signals XR_1P and XR_2P. Timing signals A, B, C, and D, along with a "read" signal, are used in a logic circuit 76, illustrated in FIG. 4, to generate timing signals

XR_1, XR_2, XR_3a, XR_3b, XR_4a, and XR_4b, which are supplied to address space selector 45. As can be seen in the schematic diagram of FIG. 5, the six timing signals are then used to operate FET switches, which supply input signals XAb_1 and XAb_2 through latches to address lines as address signals a_1i and a_2i.

[0019] The result of this timing are shown in the charts set forth below.

READ TABLE			
XAb_1	XAb_2	XR_1P	XR_2P
Bank 31	Bank 31	0	0 -> C
Bank 31	Bank 32	1	0 -> A
Bank 32	Bank 31	0	1 -> B
Bank 32	Bank 32	1	1 -> D

PROGRAM TABLE			
XAb_1	XAb_2	XR_1P	XR_2P
Bank 31	Bank 31	0	1 -> C
Bank 31	Bank 32	0	1 -> A
Bank 32	Bank 31	0	1 -> B
Bank 32	Bank 32	0	1 -> D

[0020] Thus, it can be seen that in the "read" mode, when the address represented by XAb_1 is in memory bank 31 and the address represented by XAb_2 is in memory bank 32, the designated address or location in memory bank 31 will be read or processed and, simultaneously, the designated address or location in memory bank 32 will be read or processed. Similarly, the opposite is true, that is when the address represented by XAb_1 is in memory bank 32 and the address represented by XAb_2 is in memory bank 31, the designated address or location in memory bank 32 will be read or processed and, simultaneously, the designated address or location in memory bank 31 will be read or processed. When both XAb_1 and XAb_2 represent addresses in memory bank 31 or memory bank 32, which implies that both address inputs are accessing the same memory bank. Since two addresses in a single memory core cannot be processed simultaneously, the DSP core automatically inserts a wait state and performs the XAb_1 read first and the XAb_2 read second. Inside XMRAM when both accesses are in bank 31 C goes active high and subsequently XR_3a and XR_3b go active high, where XR_3b is delayed by one instruction cycle with respect to XR_3a. This allows XAb_1 access to be read first and XAb_2 access second. A similar process takes place when both accesses are in bank 32. Programming, on the other hand, is performed only on one memory bank at a time. However, since time in a programming sequence is not as critical, the fact that a normal time is used in programming has no effect on the user.

[0021] Thus, a great speed advantage can be realized at least in DSPs, microcontrollers, or microprocessors in the ability to access, for example, instructions and data simultaneously. Further, new and improved memories in data processing equipment are disclosed which are as fast as SRAMs but non-volatile and which can be embedded in a semiconductor chip to form any of the memories associated with data processing equipment.

[0022] While I have shown and described specific embodiments of the present invention, further modifications and improvements will occur to those skilled in the art. I desire it to be understood, therefore, that this invention is not limited to the particular forms shown and I intend in the appended claims to cover all modifications that do not depart from the spirit and scope of this invention.

Claims

1. Processing equipment with embedded MRAMs characterised by:

   a data processing device (10) fabricated on a semiconductor chip; and
   MRAM cells fabricated on the chip as at least one of a data memory (15), a program or instruction memory (16), a boot memory (17), a cash memory, and controlling shift registers (11) in communication with the data processing device.

2. Processing equipment with embedded MRAMs as claimed in claim 1 wherein the MRAM cells are thin film magnetic memory cells including one of magnetic tunneling junctions (MTJ), giant magnetic resonance cells (GMR), and thin magnetic film junctions separated by an electrical conductor or an electrical insulator.

3. Processing equipment with embedded MRAMs as claimed in claim 1 wherein the MRAM cells are fabricated as a data memory and an instruction memory and the data and instruction memories include circuitry providing a dual port read function to provide simultaneous data and instruction read outputs to the data processing device.

4. Processing equipment with embedded MRAMs characterised by:

a data processing device (10) fabricated on a semiconductor chip;

MRAM cells (31,32) fabricated on the chip to form a dual bank memory in communication with the data processing device; and

circuitry coupled to the data processing device and the dual bank memory for providing simultaneous read access to the dual bank memory.

5. Processing equipment with embedded MRAMs as claimed in claim 4 wherein the dual bank data memory includes an addressable first memory bank with an output port and an addressable second memory bank with an output port and the circuitry includes first and second address inputs and logic for simultaneously routing first and second addresses on the first and second address inputs to the first and second addressable memory banks, respectively.

6. A method of fabricating data processing equipment characterised by the steps of:

fabricating a data processing device (10) on a semiconductor chip; and

fabricating MRAM cells on the chip as at least one of a data memory (15), a program or instruction memory (16), a boot memory (17), a cash memory, and controlling shift registers (11) in communication with the data processing device.

7. A method of fabricating data processing equipment as claimed in claim 6 wherein the step of fabricating MRAM cells on the chip includes fabricating an addressable dual bank data and instruction memory on the chip.

8. A method of fabricating data processing equipment as claimed in claim 7 wherein the step of fabricating an addressable dual bank data and instruction memory on the chip includes fabricating logic on the chip including first and second address inputs and logic for simultaneously routing first and second addresses on the first and second address inputs to the first and second addressable memory banks, respectively.

9. A method of fabricating data processing equipment as claimed in claim 7 wherein the step of fabricating MRAM cells on the chip includes fabricating all memories on the chip from MRAM cells.

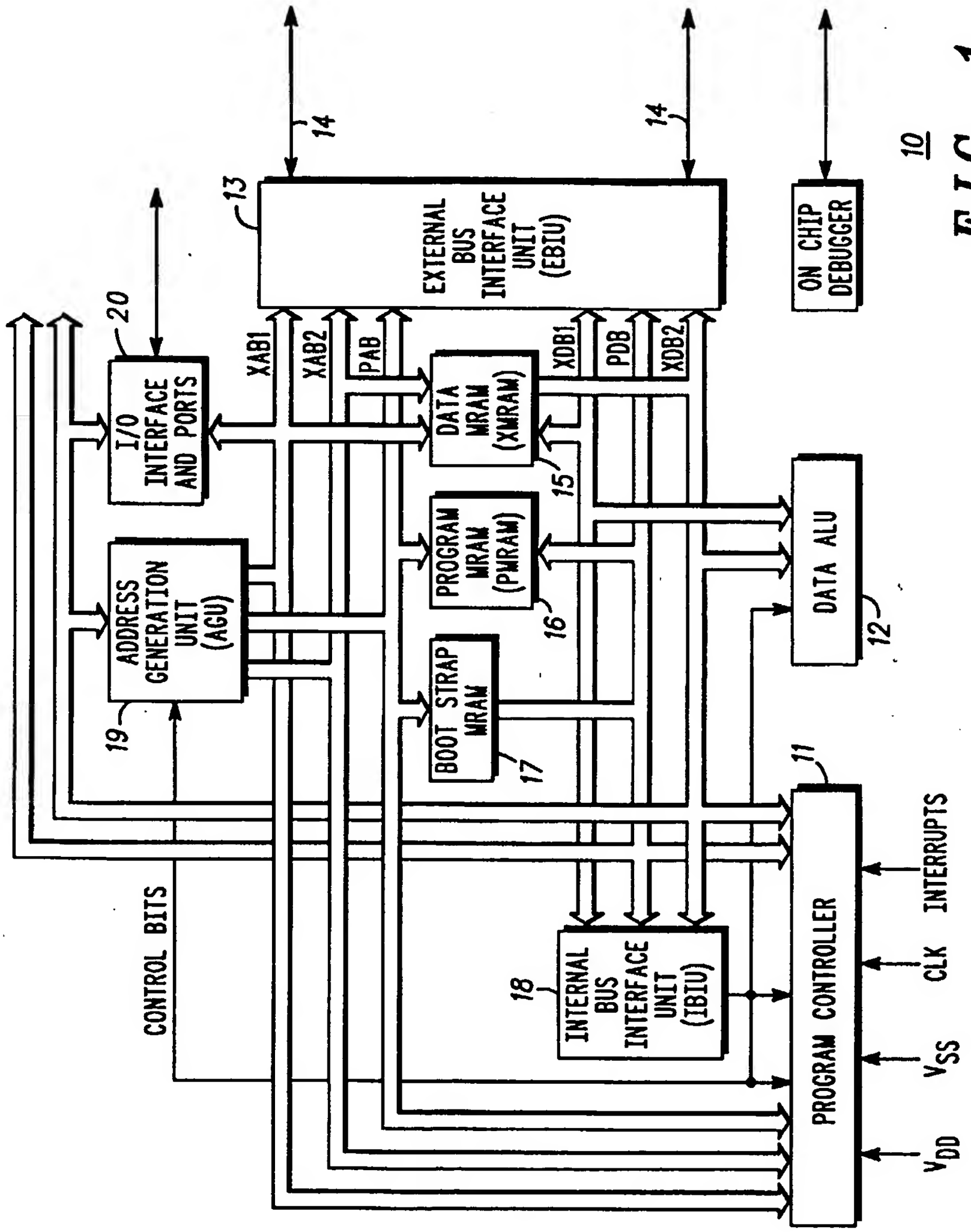
EXTERNAL BUS INTERFACE UNIT (EBIU)
13
14
14
ON CHIP DEBUGGER
10
20
I/O INTERFACE AND PORTS
XAB1
XAB2
PAB
DATA MRAM (XMRAM)
XDB1
PDB
XDB2
15
PROGRAM MRAM (PWRAM)
16
DATA ALU
12
ADDRESS GENERATION UNIT (AGU)
19
BOOT STRAP MRAM
17
11
CONTROL BITS
INTERRUPTS
18
INTERNAL BUS INTERFACE UNIT (IBIU)
PROGRAM CONTROLLER
CLK
V_{SS}
V_{DD}

FIG. 1

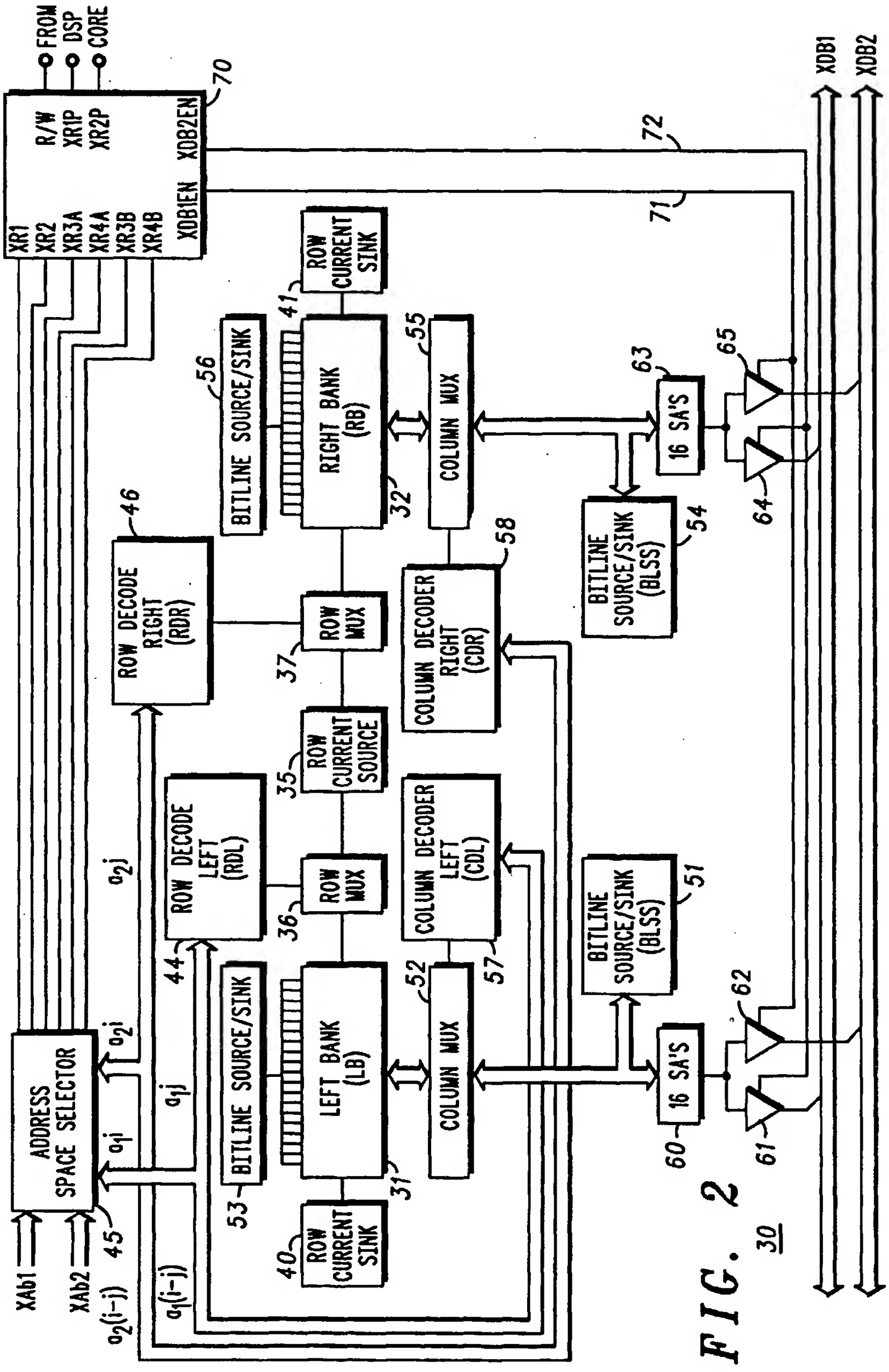
FROM
DSP
CORE
70
R/W
XR1P
XR2P
XDB2EN
XDB1EN
XR1
XR2
XR3A
XR4A
XR3B
XR4B
72
71
XDB1
XDB2
ROW CURRENT SINK
41
BITLINE SOURCE/SINK
56
RIGHT BANK (RB)
32
55
COLUMN MUX
63
16 SA'S
65
64
ROW DECODE RIGHT (RDR)
46
ROW MUX
37
COLUMN DECODER RIGHT (CDR)
58
BITLINE SOURCE/SINK (BLSS)
54
ROW CURRENT SOURCE
35
ROW DECODE LEFT (RDL)
ROW MUX
36
COLUMN DECODER LEFT (CDL)
BITLINE SOURCE/SINK (BLSS)
51
44
52
57
62
ADDRESS SPACE SELECTOR
BITLINE SOURCE/SINK
LEFT BANK (LB)
COLUMN MUX
16 SA'S
53
31
60
61
ROW CURRENT SINK
40
XAb1
XAb2
45
30

FIG. 2

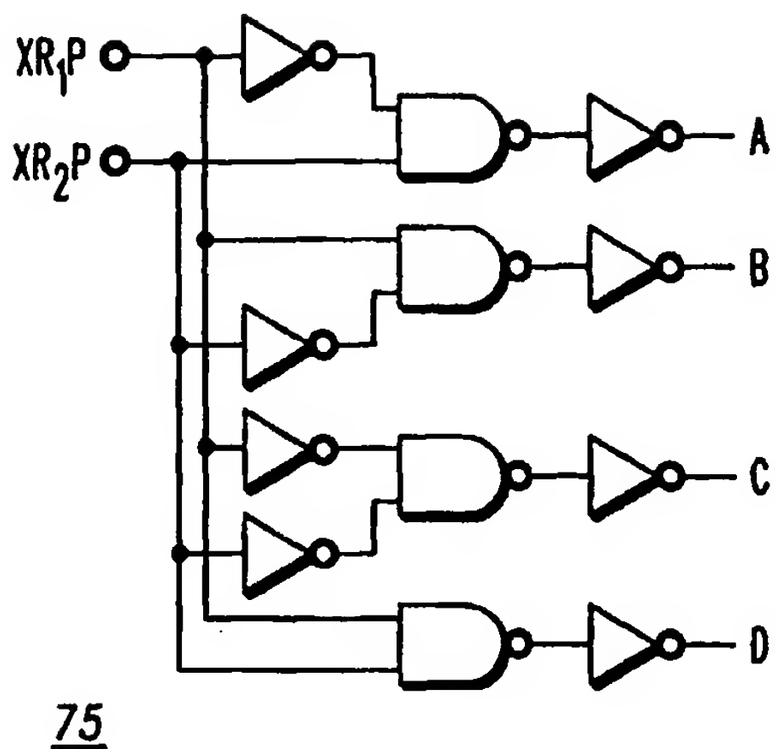

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FIG. 3

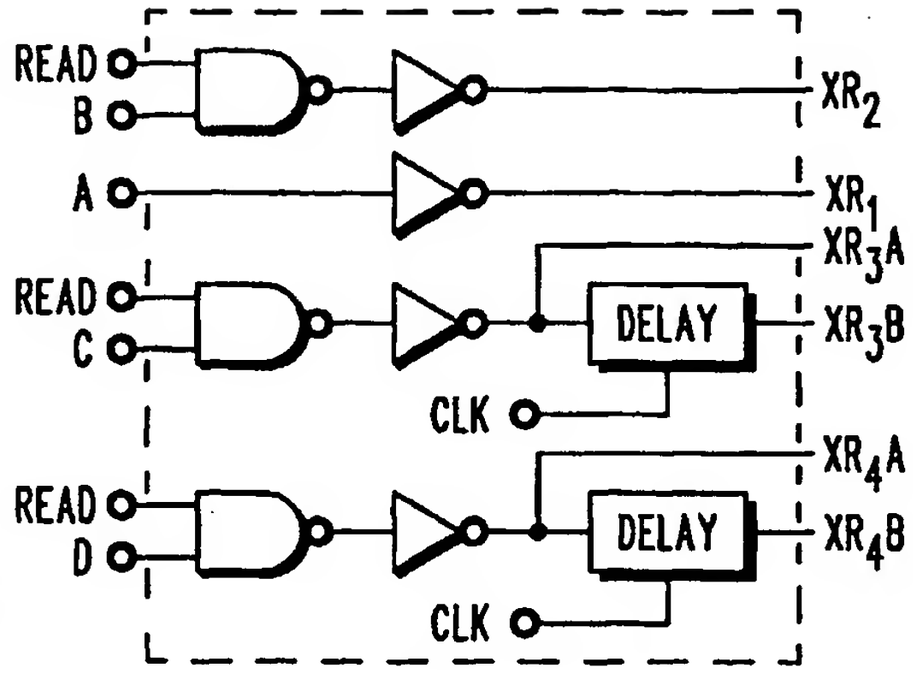

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FIG. 4

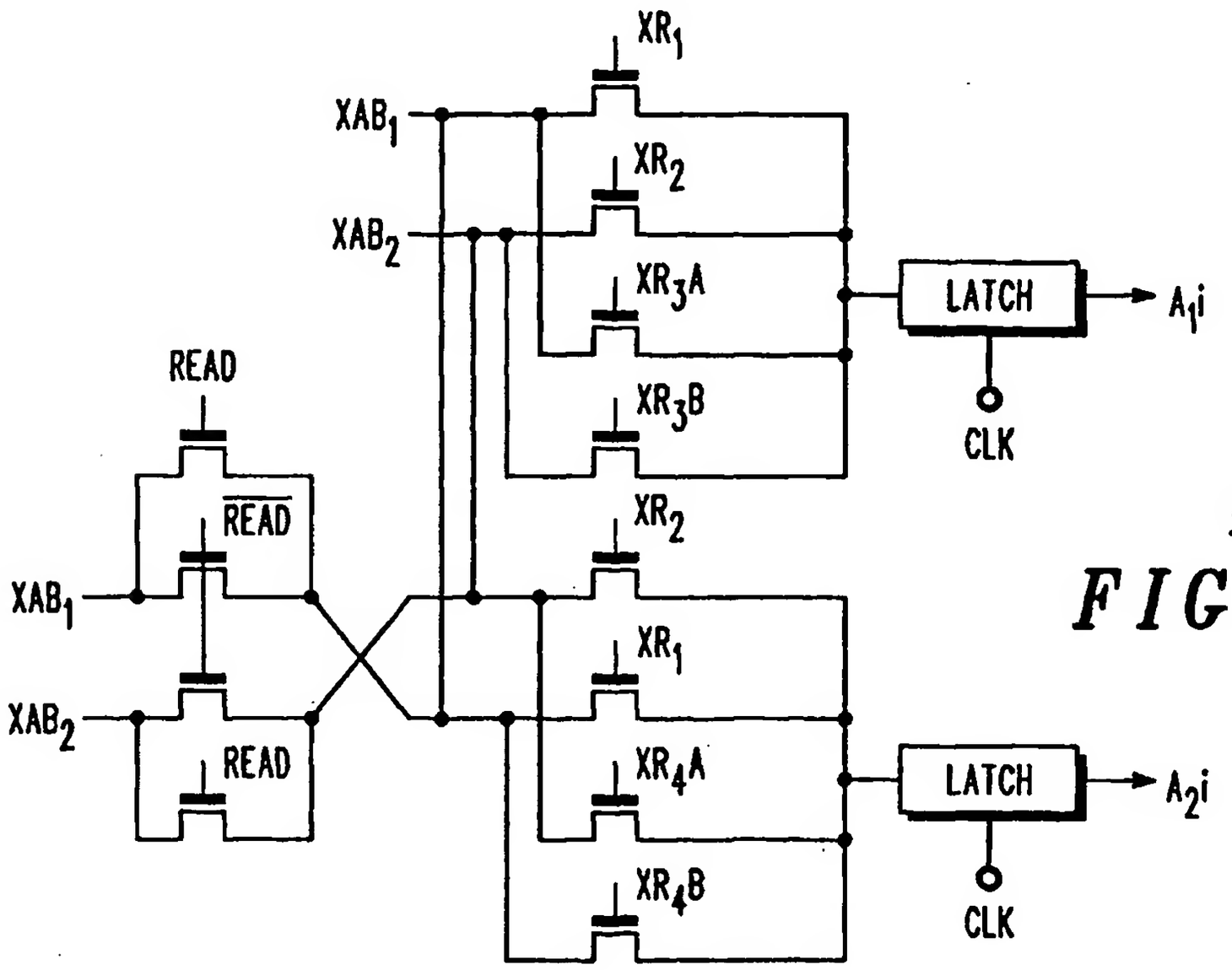

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FIG. 5

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(72) Inventor: **Naji, Peter K.**
Phoenix, Arizona 85048 (US)

(74) Representative:
Gibson, Sarah Jane et al
Motorola
European Intellectual Property Operations
Midpoint
Alencon Link
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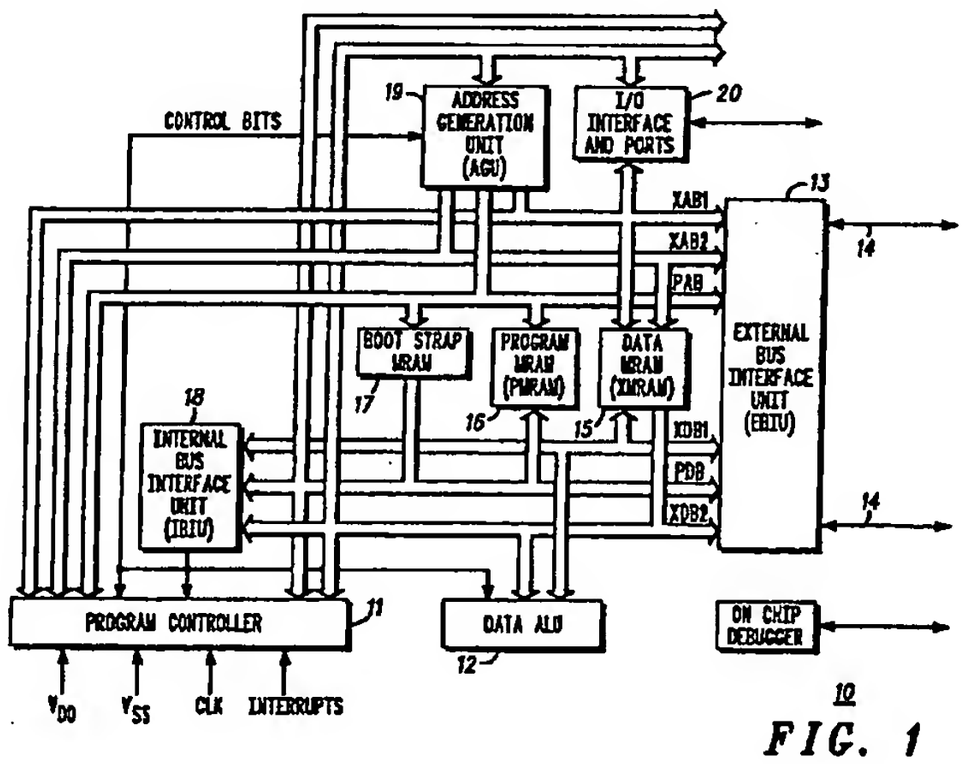

FIG. 1

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 12 2535

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WO 96 41379 A (UNIV COLUMBIA) 19 December 1996 (1996-12-19) * abstract; figure 1 *	1,6,7,9	G11C11/15 G11C8/00
A	EP 0 936 624 A (IBM) 18 August 1999 (1999-08-18) * abstract; figures 1A-1B *	1,2,6,9	
A	US 5 832 534 A (LAI KONRAD K. ET AL) 3 November 1998 (1998-11-03) * column 3, line 23 - line 44 * * column 15, line 53 - column 16, line 15; figure 4 *	1,6,9	
A	US 3 638 199 A (KOLANKOWSKY EUGENE ET AL) 25 January 1972 (1972-01-25) * column 2, line 20 - column 3, line 33 * * column 5, line 69 - column 6, line 30; figures 1,4 *	3-5,8	
A	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 11, 30 September 1998 (1998-09-30) & JP 10 162568 A (TOSHIBA CORP), 19 June 1998 (1998-06-19) * abstract * & US 6 002 631 A (HAGA) 14 December 1999 (1999-12-14) * abstract; figure 6 *	3-5,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 March 2001	Wolff, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1603 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 12 2535

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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30-03-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9641379 A	19-12-1996	NONE	
EP 0936624 A	18-08-1999	JP 11288585 A	19-10-1999
US 5832534 A	03-11-1998	US 5903908 A	11-05-1999
		US 5701503 A	23-12-1997
		US 5678020 A	14-10-1997
		US 5809524 A	15-09-1998
		US 5966722 A	12-10-1999
US 3638199 A	25-01-1972	DE 2062228 A	24-06-1971
		FR 2072166 A	24-09-1971
		GB 1316290 A	09-05-1973
		JP 49048252 B	20-12-1974
JP 10162568 A	19-06-1998	US 6002631 A	14-12-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

European Patent Office

Application Number
EP 00 12 2535

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 00 12 2535

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1,2,6,7,9

   Processing equipment on a semiconductor chip with embedded MRAMS characterised by the MRAM memory units on the chip.

2. Claims: 3,4,5,8

   Processing equipment with embedded MRAMS characterised by an MRAM dual bank memory which provides simultaneous read access.